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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/991,410	11/16/2001	Nigel G. Herron	X-915 US	3711

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EXAMINER	
TON, DAVID	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 05/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/991,410	HERRON ET AL.	
	Examiner	Art Unit	
	David Ton	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Amendment filed 12/15/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19* is/are allowed.

6)☒ Claim(s) *1-18 and 20-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Applicants Amendment filed on 12/15/2004 has been entered and reviewed.

2. Applicant's arguments with respect to claims 1-26 have been considered but are moot in view of the new ground(s) of rejection.

3. The indicated allowability of claims 20-26 are withdrawn in view of the newly discovered reference(s) to Shen et al., patent no. 6,829,751. As a result, this Office Action is maintained as a non-final Office Action.

4. Claims 1-26 are presented for examination.

Claim Rejections - 35 USC ' 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 14 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. As to claim 14, the word "**about**" on line 3 in "forming a scan chain internal to the FPGA **about** a fixed logic embedded device within the FPGA" renders the claim indefinite because the scope of the claim is unascertainable. See MPEP § 2173.05(d).

For examination purpose, the Examiner interpreted it as "forming a scan chain internal to the FPGA **to test** a fixed logic embedded device within the FPGA" .

Claim Rejections - 35 USC ' 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-18 and 20-26 are rejected under 35 U.S.C. § 103 (a) as being unpatentable over **Beebe et al.** (Beebe) patent no. **6,021,513**, in view of **Shen et al.** (Shen) patent no. **6,829,751**.

10.

11. As to claim 1, Beebe teaches the invention substantially as claimed, including a method for testing circuitry in an FPGA [see claim 6], comprising:

Configuring the FPGA for test including the FPGA forming an FPGA scan chain [see step (b) of claim 6] for simulating an external connection to an embedded device [programmable logic units of claim 6]; receiving and conducting at least one device scan chain to the embedded device [see claim 17, step d(3)]; and performing test [see claim 18, step d(4-7)].

Beebe does not teaches a fixed logic embedded device wherein the at least one device scan chain is for testing the fixed logic embedded device and further wherein the

at least one device scan chain is conducted into and through the FPGA to a scan chain logic circuit configured within the FPGA.

Shen teaches a diagnostic architecture using FPGA core in system on a chip design including configuring the FPGA [FPGA core 116 of Fig. Of Fig. 2] for test including forming scan chain [see Fig. 3] for simulating an external connection to a fixed logic embedded device [module 202a of Fig. 5] wherein the scan chain is for testing the fixed logic embedded device [specific module, col. 6 lines 45-57] and the scan chain is conducted through the FPGA [col. 6 lines 45-57].

It would have been obvious to one of ordinary skill in the Data Processing art at the time of the invention was made to combine the teachings of Beebe with the teachings of Shen to configure the FPGA scan chain as taught by Beebe for testing the fixed logic embedded device in a SOC as taught by Shen. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so because it would provide a diagnostic architecture using an FPGA core in a system on a chip (SOC) design [see Shen col. 1 lines 5-11].

12. As to claim 2, Shen teaches isolating the embedded device [col. 6 lines 45-57].

13. As to claims 3, and 4, Shen teaches transmitting/receiving at least one signal to a multiplexer [MUX 134 of Fig. 2] for delivery to the embedded device.

14. As to claim 5, Beebe teaches storing the test output signal in the scan chain [step d(5) of claim 18 (latching)].

15. As to claim 6, Beebe teaches receiving one device scan chain includes test output signals from the embedded device [see step d(6) of claim 18].

16. As to claims 7-8, Shen teaches transmitting test data to an external tester [debugging work station 104 of Fig. 2 and claim 9].

17. As to claim 9, it is similar to claim 1 above, therefore it is rejected under the same rationale. Furthermore, Shen also teaches transmitting a test signal to a MUX [MUX 134 of Fig. 2] formed within a gasket [one or more interfaces, see col. 2 lines 57-65] and transmitting the test signal from the MUX to a device under test.

18. As to claim 10, Shen teaches the device under test is an embedded core device [system on a chip of claim 1].

19. As to claim 11, Shen teaches the device under test is a fixed logic device formed within the gasket [see claim 1].

20. As to claim 12, Beebe teaches configuring the FPGA for test includes receiving an FPGA scan chain with test vectors [step 4(d) of claim 18].

21. As to claim 13, Shen teaches receiving and conducting at least one device scan chain to the device under test [see Fig. 3].

22. As to claim 14, it is similar to claim 1 above, therefore it is rejected under the same rationale. Furthermore, Shen also teaches transmitting a test signal to a MUX [MUX 134 of Fig. 2] formed within a gasket [one or more interfaces, see col. 2 lines 57-65] and transmitting the test signal from the MUX to a device under test.

23. As to claims 15-18, they are similar to claims 10-13, therefore, they are rejected under the same rationale.

24. As to claim 20, it is similar to claim 1 above, therefore it is rejected under the same rationale. Furthermore, Shen also teaches a Gasket [I/O port 132 of Fig. 2] formed at least partially within the FPGA fabric portion, the Gasket forming interfacing logic between an embedded core device and the fabric portion [see claim 1]; and at least one multiplexer [MUX 134 of Fig. 2] coupled serially between the FPGA fabric portion and the embedded core device.

25. As to claims 20-26, Shen teaches the multiplexer [MUX134 of Fig. 2] is coupled to receive outputs from a fixed logic device formed within the gasket.

Allowable Subject Matter

26. Claim 19 is allowed.

Response to Remarks

27. Applicants argued that Crouch at al. filed their application after the present application was filed and it can not be used as prior art.

Crouch patent is not used in this rejection. However, the Examiner need to point out to the Applicants that the Crouch's patent had been filed seven years before the present application was filed (September 1994 compare with November 2001). Therefore, the previous rejection was proper.

Conclusion

28. The prior art of record and not relied upon is considered pertinent to applicant's disclosure.

29. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Ton whose telephone number is (571) 272-3828. The examiner can normally be reached on M-Th from 5:30 - 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David Ton
Primary Examiner
Art Unit 2133